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B028312(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

(AICTE Scheme)

(Electronics & Telecommunication Engineering Branch)

ELECTRONICS DEVICES

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

***Note** : All questions are compulsory. Part (a) of each question is compulsory and attempt any two parts from parts (b), (c) and (d). Part (a) is of 4 marks and part (b), (c) and (d) each are of 8 marks. Assume suitable data whenever required.*

Unit-I

1. (a) A potential difference of 10 V is applied longitudinally to a rectangular speciman of intrinsic germanium of length 25 mm, width 4 mm and thickness 1.5 mm. Find the total current if intrinsic carrier concentration

is $2.5\times10^{19}/m^3$, $\mu_e = 0{\cdot}38\,m^2\ V^{-1}s^{-1}$, $\mu_h = 0{\cdot}18\ m^2V^{-1}s^{-1}$.

(b) Draw the energy band diagram of an open circuited p-n junction. Indicate Fermi level and contact potential E_0?

(c) In intrinsic GaAs, the electron and hole mobilities are 0.85 and 0.04 m^2/V-s respectively and corresponding effective masses are 0.068 m_0 and 0.5 m_0 respectively where m_0 is the rest mass of an electron. If the energy gap of GaAs at 300 K is 1.43 eV, calculate the intrinsic carries concentration and conductivity.

(d) Derive the following expression for a step graded junction $V_0 = V_T \log_e \left(\frac{N_A N_A}{n_i^2}\right)$.

Unit-II

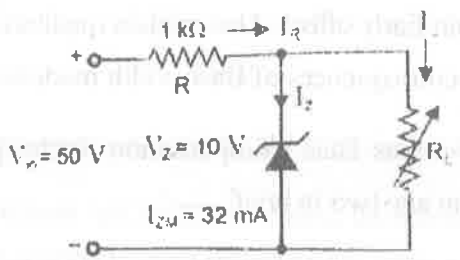
2. (a) (i) Define ripple factor and transformer utilization factor.

(ii) Why π -filters are not suitable for varying loads?

(b) Describe bridge rectifier. How does it differ from full wave rectifier using two diodes only? What do you understand by PIV?

(c) Explain the working of zener diode as a voltage regulator?

(d) For the network shown in below figure, determine the range of RL and IL that will result in VRL being maintained at 10 V, also determine the maximum wattage rating of diode.



Unit-III

3. (a) Explain following terms :

(i) Operating Point

(ii) Punch through

(iii) Thermal Runaway

(iv) Advantage of CE over CB and CC

(b) (i) Draw and explain the current components in a pnp transistor?

(ii) For a certain npn transistor $I_C = 5$ mA, $I_B = 50$ μA and $I_{CBO} = 1\mu A$.

Calculate α, β and I_E. Determine the new level of I_B required to make $I_C = 10$ mA.

(c) Explain Early effect. Also explain qualitatively the three consequences of Base width modulation?

(d) List various Bias Compensation Technique and explain any two in brief.

Unit-IV

4. (a) (i) Why FET is called a voltage controlled device?

(ii) Explain why does the drain current I_D not reduced to zero even after the channel is pinched off?

(b) Explain drain characteristics of n-channel JFET. Explain shape of characteristics and identify regions.

(c) (i) Compare JFET with BJT.

(ii) Why input impedance of FET is high?

(iii) Obtain the expression for the Pinch OFF voltage V_P in case of n-channel JFET?

(d) An n-channel JFET has $I_{DSS} = 10$ mA and pinch off voltage $V_P = -4$ V. Find the drain current for $V_{GS} = -2$ V. If transconductance g_m of a JFET with the same I_{DSS} at $V_{GS} = 0$ V is 4 m Mho, find the pinch off voltage.

Unit-V

5. (a) Explain working of MOSFET as a switch.

(b) (i) Which MOSFET is called as Normally ON MOSFET and NORMALLY OFF MOSFET and why?

(ii) Make comparison between JFET and MOSFET.

(c) Define Pinch OFF voltage, threshold voltage and draw drain characteristics and tansfer characteristics for *n*-channel *E* MOSFET.

(d) Determine I_{DQ} and V_{DSQ} for Enhancement type MOSFET for given circuit.